Key Challenges

- Non-uniform and complex routing track configuration
- Need to route in between small obstacles
- Maintain the topology consistency for all the bits in the same bus

Evaluation Rule

Routing Cost
- Wire length cost: shorter \(\rightarrow\) better
- Segment cost: less \(\rightarrow\) better
- Compactness cost: more compact \(\rightarrow\) better

Penalty Cost
- Spacing violation penalty
- Routing failure penalty
- Wire off-track
- Track width violation
- Bit open
- Topology inconsistency

MARCH: MAze Routing

Under a Concurrent and Hierarchical Scheme for Buses

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Two Key Features of MARCH
- Hierarchically \(\rightarrow\) Efficiency
- Concurrently \(\rightarrow\) Correct-by-construction

Experimental Results

MARCH Details of MARCH on IC/CAD 2018 Benchmarks

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Menu/Weights</th>
<th>MARCH Scores</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wire length</td>
<td>Shorter</td>
<td>Better</td>
</tr>
<tr>
<td>Segment number</td>
<td>Less</td>
<td>Better</td>
</tr>
<tr>
<td>Compactness</td>
<td>More compact</td>
<td>Better</td>
</tr>
</tbody>
</table>

Track Assignment for Bits (TAB)
- Track segment range estimation
- Exact track selection
- Exact track segment range assignment

Experimental Results

MARCH

Topological Path Planning (TAP)
- Same layer propagation
- Layer switching
- Build routing paths for multi-pin buses

See image of MARCH and TAB for visual representation.