# Dr. CU: Detailed Routing by Sparse Grid Graph and Minimum-Area-Captured Path Search

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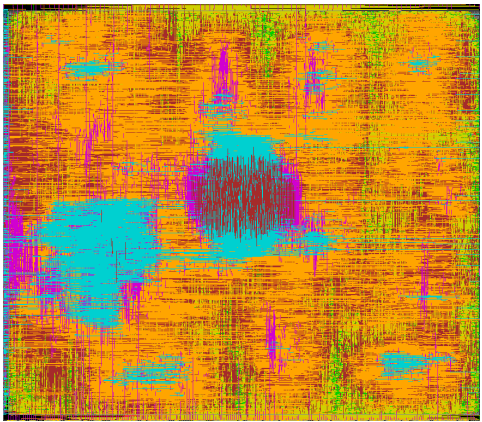
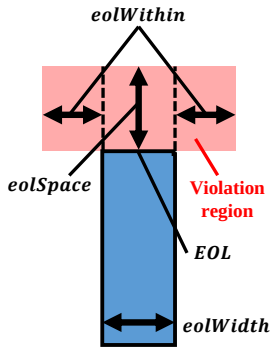
# Introduction – Key Challenges of Detailed Routing

- Compared to global routing
  - On a significantly larger solution space ($10^4 \times 10^4 \times 10$ grid graph)
  - Has many design rules
- Even more time-consuming and complicated in advanced tech nodes

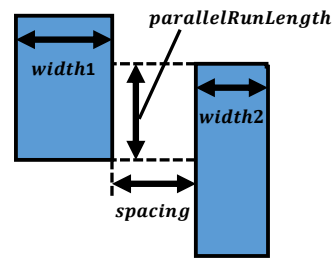


# Introduction – Design Rules

- Short
- Spacing: parallel-run spacing, EOL spacing, cut spacing, ...
- Min area




(a) EOL spacing




(b) Parallel-run spacing

# Introduction – Problem Formulation of Detailed Routing

Given

- Placed netlist
- Routing guides (from global routing)
- Routing tracks
- Design rules

Route all the nets & minimize a weighted sum of

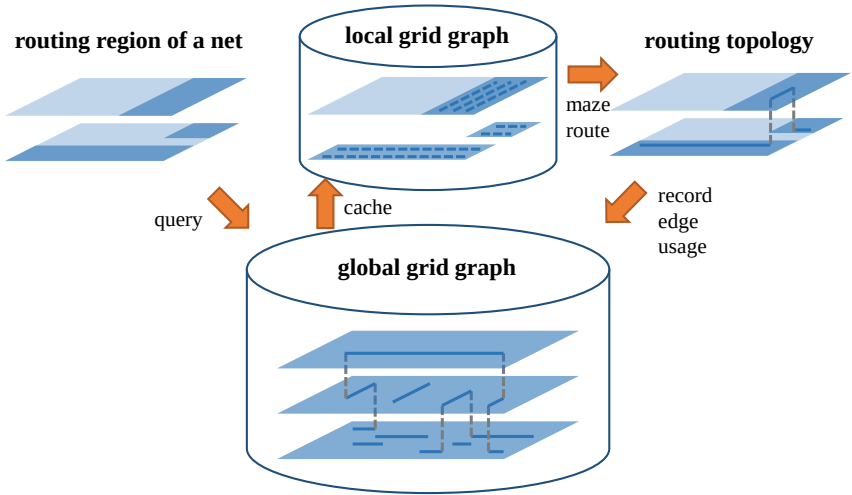
- Total wire length
- Total via count
- Non-preferred usage (including out-of-guide & off-track wires/vias, wrong-way wires)
- Design rule violations

# Introduction – Our Approach

- Two-level sparse data structures $\Longrightarrow$ efficiency
- Min-area-captured path search $\Longrightarrow$ quality
- Bulk synchronous parallel $\Longrightarrow$ further speed-up

# Outline

# Two-Level Sparse Data Structures

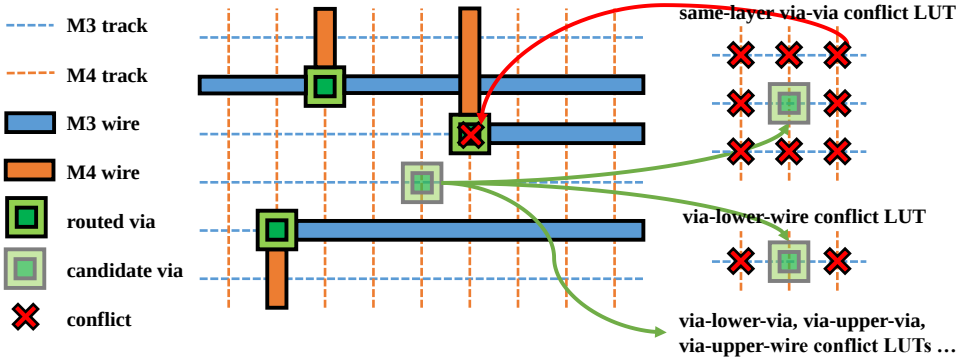


# Sparse Global Grid Graph

- Store routed edges by BSTs & intervals
- Query via/wire conflict efficiently with help of LUTs
  - Support batch query

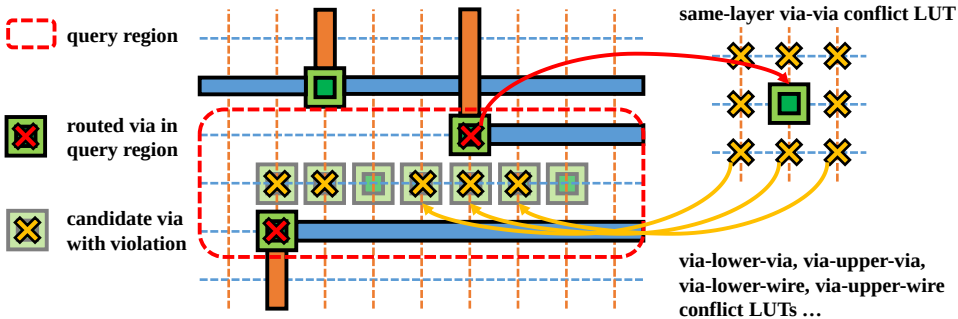
# Sparse Global Grid Graph

Example: query the conflict with a single candidate via



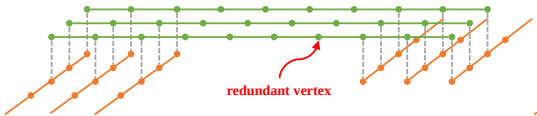
# Sparse Global Grid Graph

Example: query the conflict with many neighboring candidate vias



# Sparse Local Grid Graph

- Cache global graph on routing region
  - Subgraph of full-chip grid graph on routing region of a net
  - Store vertex/edge information explicitly by direct-address tables
- Remove redundant vertices




(a) Before removing redundant vertices

(b) After removing redundant vertices

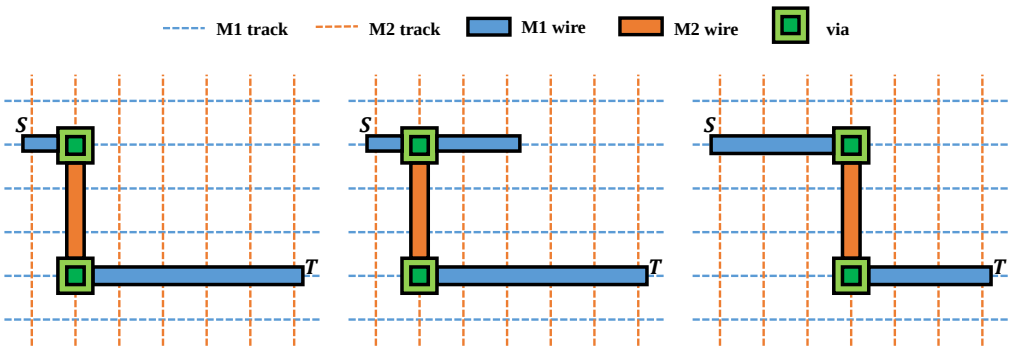
# Sparse Local Grid Graph

- Edge cost in local grid graph captures
  - Base wire & via cost
  - Out-of-guide penalty
  - Short & spacing violation penalty
- How about min-area violation?

# Outline

# Min-Area-Captured Path Search

Capture min area cost in path search (without considering wire extension)




(a) A normal path search without considering min-area violation

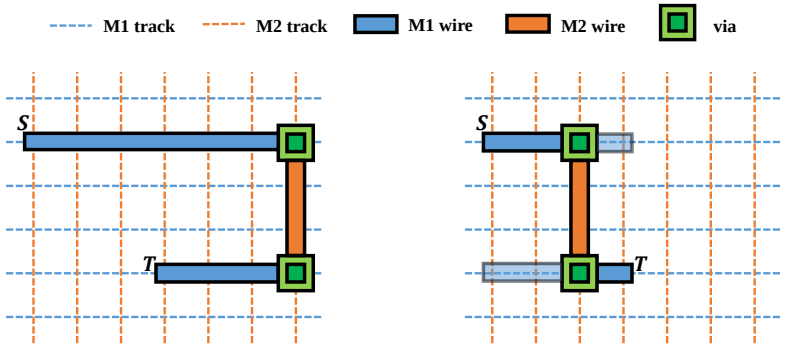
(b) Post fixing by extending wire

(c) Forcing the min length of wire segment in path search

(Suppose the min area rule implies a length of three pitches)

# Min-Area-Captured Path Search

Capture min area cost in path search (with wire extension considered)




(d) Detour due to the forcing

(e) Path search with wire extension considered

# Min-Area-Captured Path Search

Normal Dijkstra's algorithm

- Cost/distance that can be directly incremented
  - $cost(v_1 \rightsquigarrow v_2 \rightsquigarrow v_3) = cost(v_1 \rightsquigarrow v_2) + cost(v_2 \rightsquigarrow v_3)$
- A vertex is visited at most once
- Back track by each vertex having a prefix

Min-area-captured path search

- Uncertain cost
  - Lower bound: edge cost sum + min-area penalty on **previous wires**
  - Upper bound: lower bound + min-area penalty on the **current wire**
- A vertex may be visited multiple times
- Back track by (smart) pointers

# Outline

# Bulk Synchronous Parallel

- Route batches of independent nets one after another
- Fast scheduling followed by load balancing

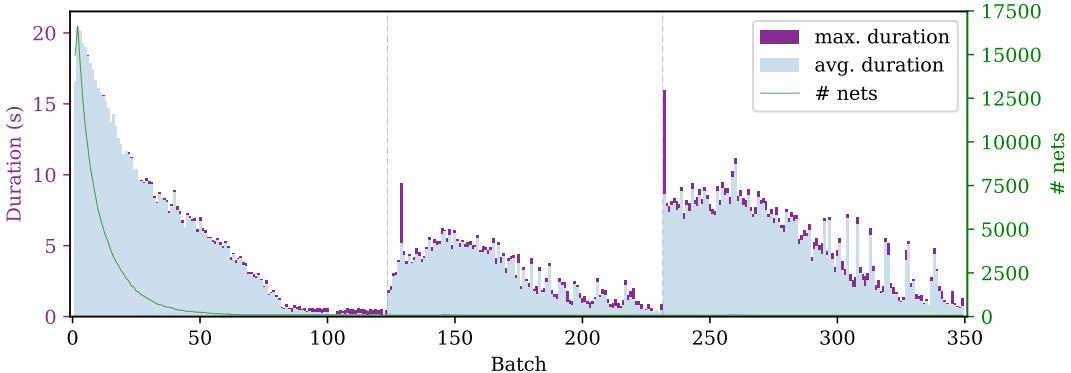



Figure: Scheduling without load balancing

# Bulk Synchronous Parallel

- Route batches of independent nets one after another
- Fast scheduling followed by load balancing

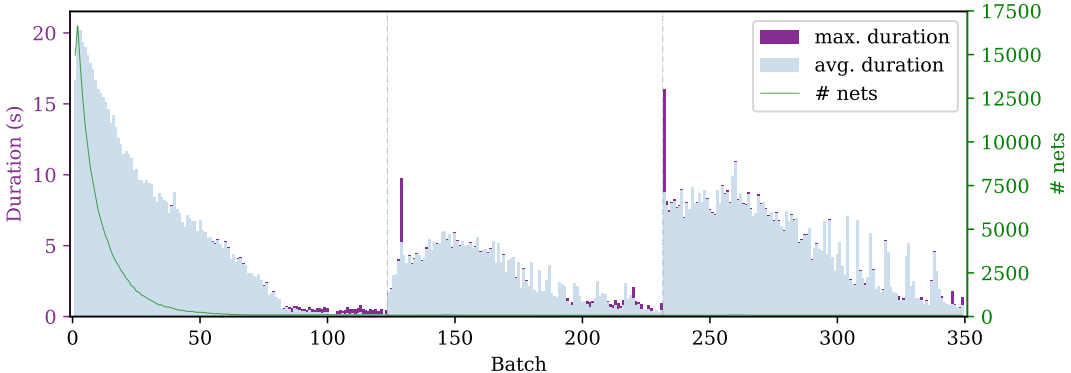



Figure: Scheduling with load balancing

# Bulk Synchronous Parallel

- Separate a batch into **routing** and **committing** phases

| | Routing phase | Committing phase |
|---|---|---|
| domain | whole routing region | solution paths |
| global grid graph access | read | write |
| locked? | lock-free | locked |

# Outline

# Experimental Results

- On ISPD 2018 Contest Benchmarks

| Benchmark | # std. cells | # block macros | # nets | # pins | # IO pins | # layers | M2 # tracks | M2 pitch ($\mu$m) | Tech. node (nm) |
|---|---|---|---|---|---|---|---|---|---|
| test1 | 8879 | 0 | 3153 | 17203 | 0 | 9 | 977 | 0.2 | 45 |
| test2 | 35913 | 0 | 36834 | 159201 | 1211 | 9 | 3254 | 0.2 | 45 |
| test3 | 35973 | 4 | 36700 | 159703 | 1211 | 9 | 4943 | 0.2 | 45 |
| test4 | 72094 | 0 | 72401 | 318245 | 1211 | 9 | 8886 | 0.1 | 32 |
| test5 | 71954 | 0 | 72394 | 318195 | 1211 | 9 | 9800 | 0.1 | 32 |
| test6 | 107919 | 0 | 107701 | 475541 | 1211 | 9 | 5312 | 0.1 | 32 |
| test7 | 179865 | 16 | 179863 | 793289 | 1211 | 9 | 13500 | 0.1 | 32 |
| test8 | 191987 | 16 | 179863 | 793289 | 1211 | 9 | 13500 | 0.1 | 32 |
| test9 | 192911 | 0 | 178857 | 791761 | 1211 | 9 | 13500 | 0.1 | 32 |
| test10 | 290386 | 0 | 182000 | 811761 | 1211 | 9 | 13500 | 0.1 | 32 |

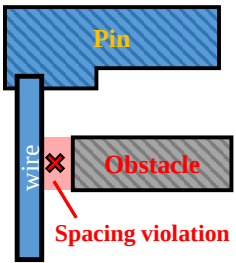
# Experimental Results

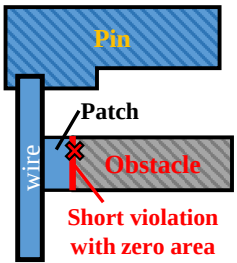
- On ISPD 2018 Contest Benchmarks

| Metric | | Weight |
|---|---|---|
| wire length | | 0.5 |
| # vias | | 2 |
| non-preferred usage | out-of-guide wire length | 1 |
| | # out-of-guide vias | 1 |
| | off-track wire length | 0.5 |
| | # off-track vias | 1 |
| | wrong-way wire length | 1 |
| design rule violations | short metal area | 500 |
| | # spacing violations | 500 |
| | # min-area violations | 500 |

# Experimental Results

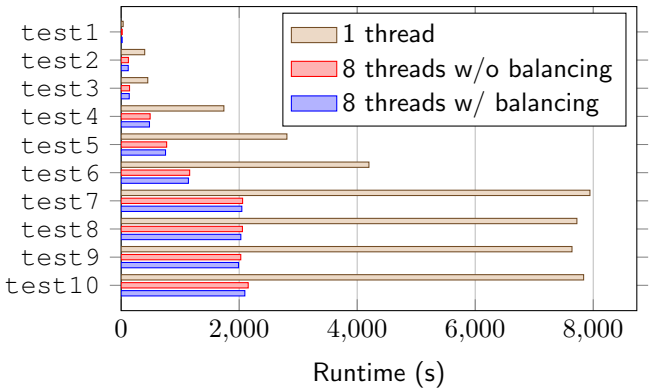
- We do not abuse contest metric by converting spacing violations into short ones with zero area.



# Experimental Results

- 8 threads gives almost $4\times$ speed-up
- Load balancing contributes 2.52% improvement



# Experimental Results

| | | WL | # vias | Non-preferred usage | | | | | Design rule violations | | | | | Quality score | Mem (GB) | Time (s) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Out-of-guide | | Off-track | | Wrong-way | # | Short | # | # min | Total | | | |
| | | | | WL | # vias | WL | # vias | WL | short | area | spacing | area | # | | | |
| Metric weight | | 0.5 | 2 | 1 | 1 | 0.5 | 1 | 1 | - | 500 | 500 | 500 | - | - | - | - |
| Dr. CU | test1 | 434914 | 34443 | 4352 | 859 | 276 | 0 | 2363 | **127** | 15 | 122 | 0 | **249** | **362725** | **0.32** | **17** |
| | test2 | 7817285 | 339055 | 104720 | 11784 | 4353 | 0 | 22023 | **1005** | 1330 | 1949 | 0 | **2954** | 6366886 | **1.15** | **121** |
| | test3 | 8707641 | 331958 | 176736 | 10731 | 4344 | 0 | 22187 | **2444** | 1982 | 2419 | 0 | **4863** | **7430092** | **1.25** | **139** |
| | test4 | 26042785 | 701994 | 769265 | 31444 | 41791 | 0 | 89537 | **6914** | 26329 | 11224 | 0 | **18138** | **34112928** | **2.89** | **494** |
| | test5 | 27852167 | 942588 | 649224 | 43071 | 13390 | 0 | 63397 | **5466** | 4722 | 7742 | 0 | **13208** | **22805761** | **3.87** | **767** |
| | test6 | 35813473 | 1446807 | 976672 | 68656 | 20357 | 0 | 95811 | **7959** | 12891 | 11023 | 0 | **18982** | **33908653** | **5.16** | **1155** |
| | test7 | 65360688 | 2349580 | 2187794 | 101866 | 33105 | 0 | 170316 | **23141** | 33041 | 14880 | 0 | **38021** | **63816462** | **8.86** | **2071** |
| | test8 | 65668468 | 2360231 | 2288159 | 102982 | 33373 | 0 | 170583 | **20641** | 22353 | 14384 | 0 | **35025** | **58501486** | **8.92** | **2060** |
| | test9 | 54993356 | 2358857 | 1604576 | 115465 | 29620 | 0 | 168722 | **18830** | 17316 | 14470 | 0 | **33300** | **50010785** | **8.52** | **2016** |
| | test10 | 68282001 | 2532666 | 2826908 | 140343 | 32865 | 0 | 180586 | **26688** | 150705 | 20837 | 0 | **47525** | **128141527** | **8.98** | **2132** |
| | **Avg. ratio** | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 | - | 1.00 | **1.00** | 1.00 | 1.00 | - | **1.00** | **1.00** | **1.00** | **1.00** |
| 1st place of ISPD 2018 | test1 | 472032 | 41641 | 6246 | 1385 | 3528 | 116 | 3509 | 4223 | 1 | 107 | 0 | 4330 | 386188 | 4.64 | 207 |
| | test2 | 8150588 | 409551 | 71685 | 13451 | 20402 | 1362 | 18214 | 36601 | 95 | 1158 | 1 | 37760 | **5636274** | 32.55 | 1514 |
| | test3 | 9086139 | 427410 | 69182 | 2450 | 33470 | 1216 | 18882 | 46966 | 4891 | 1387 | 0 | 48353 | 8645534 | 43.40 | 2019 |
| | test4 | 27514053 | 858224 | 240226 | 8841 | 150961 | 1011 | 224715 | 349597 | 52947 | 50957 | 6 | 400560 | 67978777 | 46.52 | 4706 |
| | test5 | 29151781 | 1140804 | 309785 | 30902 | 45523 | 10656 | 193203 | 418235 | 28199 | 66250 | 22 | 484507 | 64660336 | 24.25 | 1914 |
| | test6 | 37987679 | 1775407 | 467961 | 42448 | 153900 | 17644 | 281060 | 626956 | 30949 | 100229 | 12 | 727197 | 89025895 | 28.40 | 3107 |
| | test7 | fail | fail | fail | fail | fail | fail | fail | fail | fail | fail | fail | fail | fail | fail | fail |
| | test8 | 69559382 | 2929578 | 1006247 | 82478 | 375236 | 22294 | 455824 | 1058138 | 76790 | 161229 | 48 | 1219415 | 161426598 | 41.81 | 6262 |
| | test9 | 58803453 | 2920259 | 813750 | 67367 | 331766 | 22915 | 446432 | 1051112 | 56581 | 158305 | 40 | 1209457 | 144221466 | 40.16 | 5128 |
| | test10 | 72244024 | 3110163 | 1414338 | 81831 | 625291 | 27392 | 476670 | 1289359 | 120966 | 177426 | 33 | 1466818 | 193867714 | 45.15 | 5554 |
| | **Avg. ratio** | 1.06 | 1.23 | 0.58 | 0.73 | 9.02 | - | 2.18 | 50.32 | 2.28 | 6.10 | - | 26.70 | 1.97 | 13.27 | 6.89 |

# Experimental Results

Compared with 1st place of ISPD Contest

- 35% better routing quality under contest metric
  - 5% less wire length and 19% fewer vias
  - 3.7× design rule violation clearance
- 26.7× reduction in number of design rule violations
- 80% - 93% memory reduction
- 2.5× - 15× speed-up

# Experimental Results

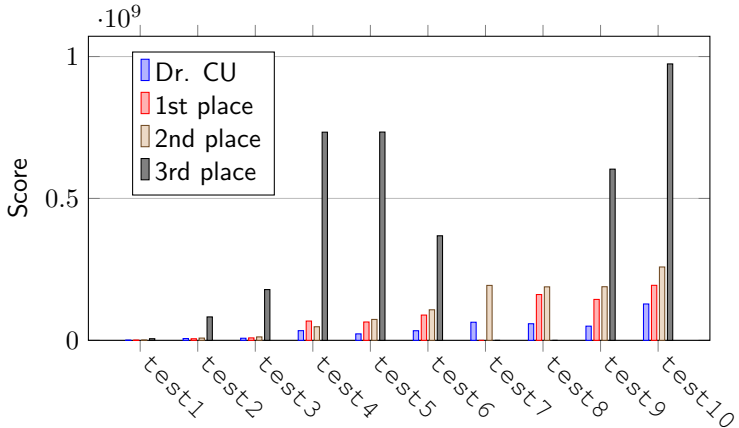



Figure: Comparison on quality score under the metric of ISPD 2018 Contest*

*1st place fail in `test7`, 3rd place fail in `test7` & `test8`

# Experimental Results

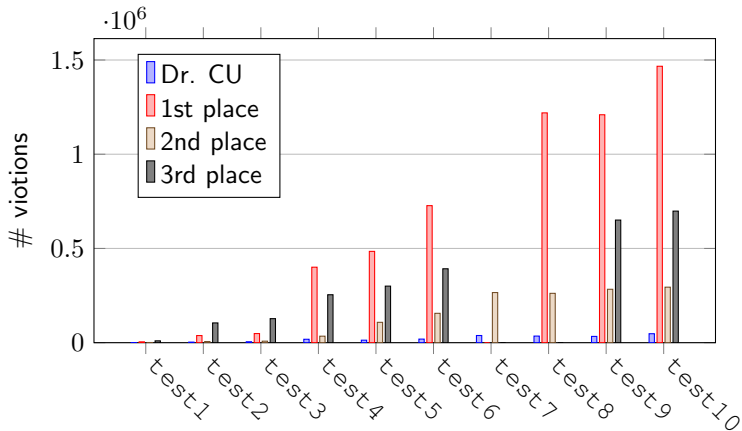



Figure: Comparison on total number of short, minimum area, and spacing violations

# Experimental Results

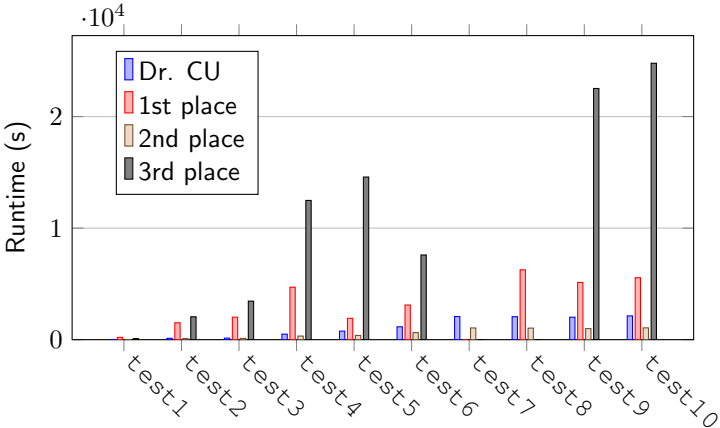



Figure: Comparison on runtime

# Conclusion

Our approach

- Two-level sparse data structures $\Longrightarrow$ efficiency
- Min-area-captured path search $\Longrightarrow$ quality
- Bulk synchronous parallel $\Longrightarrow$ further speed-up

A stronger Dr. CU? To be published...

- Shorter wire length, fewer vias
- Significantly fewer design rule violations (by 1–2 orders of magnitudes)
- Faster